REMARKS/ARGUMENTS

In the Office Action, claims 14-16 were initially rejected under 35 U.S.C. §102(b) as being anticipated by Kikushima, et al. (U.S. Patent 5,410,173).

Claim 14 Issues:

Claim 14 has been amended as shown above to recite that at least one row of the standard cell array has spacing between cells. The cited reference to Kikushima notes in column 11, lines 1-6, that it is talking about a sea of gates system in which the cells arre arranged in a matrix without any space between them. Furthermore, this reference notes that it is unlike the "fixed channel type" and therefore does not include channel regions between the rows themselves. Notably, the applicant's specification supports spacing between cells (as well as between rows of cells). For example, Fig. 6 shows that the third row of cells contains spaced apart cells. Thus, it is believed that claim 14 is different from the cited reference. Furthermore, it is noted that the cited reference teaches away from the applicant's spacing and thus, would not serve as a §103 reference. Therefore, applicant believes that claim 14 is in condition for allowance.

Claim 15 Issues:

Claim 15 recites "a pair of power conductors extending across cells of said standard cell array and cells of said macro region". The cited reference (5,410,173) to Kikushima indicates that different power conductors are utilized for the cells in the standard cell array region and for cells in a macro. For example, in column 17, at lines 40-43, the Kikushima specification indicates that power to the logic cells of the standard cell array is supplied through wiring of the third layer, namely, busses 164A and 164B, as well as wiring of the second layer though busses 165A and 165B. Furthermore, Kikushima notes that at column 18, lines 42-45 that power is supplied to the macro block through bus 196 and 198. Thus, it is apparent that the Kikushima reference does not teach a pair of power conductors extending across cells of the standard cell array and cells of the macro region. Rather, different power conductors are utilized for the cells in the standard cell array region and for cells in the macro region. Thus, it is believed that claim 15 is in condition for allowance.

Claim 16 Issues:

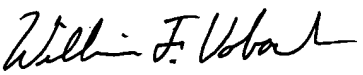
Claim 16 has been amended to recite that the parallel power conductors running adjacent all of the cells of a standard cell array and the cells of the macro are in the same level of the integrated circuit. As noted above, the Kikushima reference indicates that the power conductors for the logic cells are disposed in both the second and third layer and that power supply wiring for the macro is disposed in the second layer. Claim 16, thus is different from the Kikushima reference in that the power conductors running adjacent the cells are in the same level of the integrated circuit. Thus, it is believed that claim 16 is in condition for allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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